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MEG2000-012

29 August 2002

To: Commissioner of Patents and Trademarks
Washington, DC 20231

ATTN: Group Art Unit: 2811 COSTANZO, PATRICIA M.

From: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, NY 12603

Serial No. 09/821,546 03/30/2001
JIN-YUAN LEE

A STRUCTURE AND MANUFACTURING METHOD OF CHIP SCALE PACKAGE

Group Art Unit: 2811 COSTANZO, P. M.

RESPONSE PATENT OFFICE ACTION

Dear Sir:

In response to the Office Action dated 06/03/02, please amend the above-identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patent and Trademarks, Washington, DC 20231, on September 3, 2002.

Stephen B. Ackerman, Reg. No: 37,761

Signature

Date September 3, 2002

AMENDMENT

The Commissioner is hereby authorized to charge payment of any additional fees involved with added Claims and the like to Deposit Account No. 19-0033.

IN THE SPECIFICATION

Please replace the second paragraph on page 10 with the rewritten following paragraph:

A1

It is also known in the art that chip sites are first formed on a semiconductor substrate to form a wafer, where the substrate is provided with pads (110/115) or (140/115) that are connected to underlying multi-level metal layers through intervening insulating dielectric layers, and ultimately to integrated circuit devices that have already been conventionally formed within and on the substrate. These conventional steps are well known in the art and as they are not significant to the invention, they are not described in detail here in order not to unnecessarily obscure the present invention. However, it is described below in the embodiments of the present invention a new method of forming a chip scale package (CSP) where the I/O